

1/18

FIG. 1A

PRIOR ART

<code>_asm int uci(int_reg_src, unsigned char_imm);</code> (F91)
<code>⋮</code>	
<code>a = uci(b, 255);</code> (T91)
<code>⋮</code>	
<code>a = (b+10) & 255;</code> (T92)

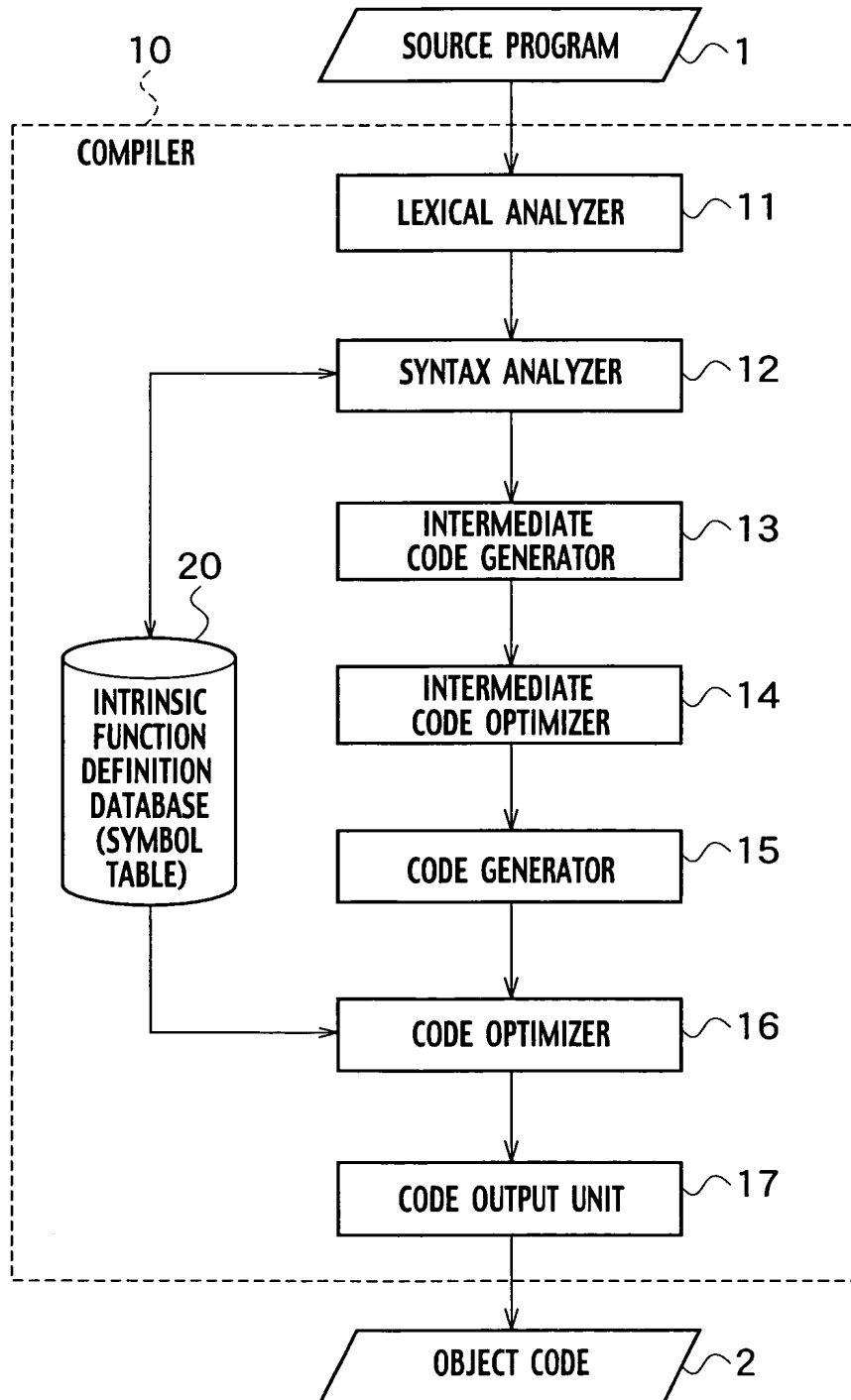
FIG. 1B

PRIOR ART

<code>uci \$0, \$1, 255</code> (M91)
<code>⋮</code>	
<code>add \$3, \$1, 10</code>	} (M92)
<code>add \$0, \$3, 255</code>	

2/18

FIG. 2



3/18

FIG. 3

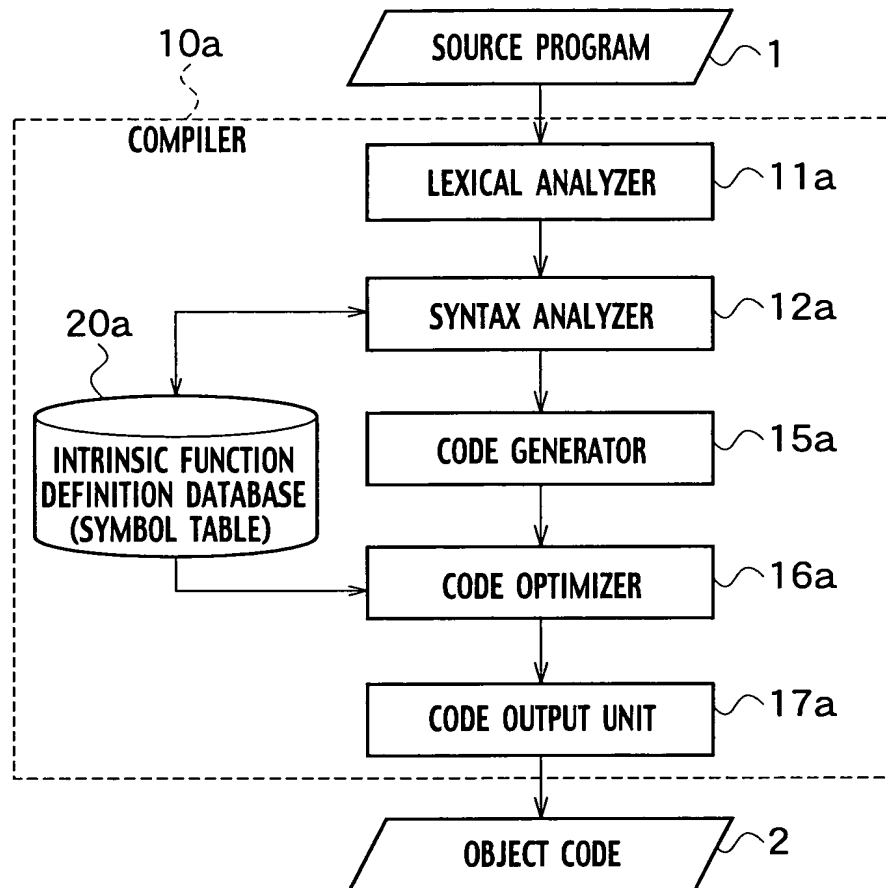
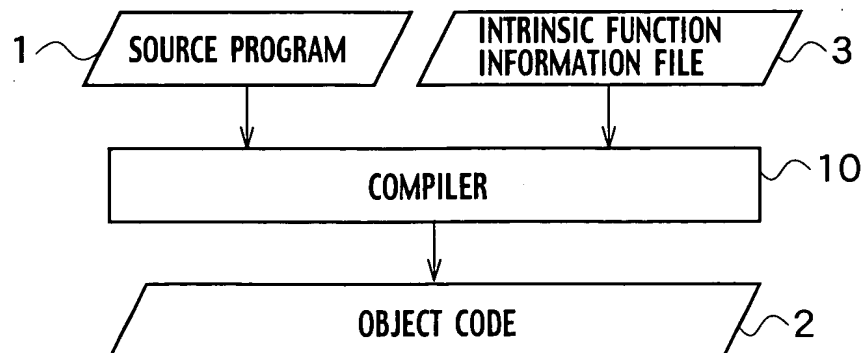


FIG. 4



4/18

FIG. 5A

```
/* DEFINITION OF INTRINSIC FUNCTION (#num1) */  
_asm int uci(int_reg_src, unsigned char_imm) {  
    return (_reg_src + 10) &_imm;  
}
```

P11

F11

FIG. 5B

```
/* DEFINITION OF INTRINSIC FUNCTION (#num2) */  
_asm int uci(int_reg_src, unsigned char_imm) {  
    int tmp = _reg_src + 10;  
    tmp &= _imm;  
    return tmp;  
}
```

P12

F12

5/18

FIG. 6A

/* EXPLICIT CALL OF INTRINSIC FUNCTION */	
int a, b;	
a = uci(b, 255);(T11)
a = uci(a, 127);(T12)

FIG. 6B

uci \$0, \$1, 255(M11)
uci \$0, \$0, 127(M12)

6/18

FIG. 7A

int a, b;	
a = (b+10) &255;(T21)
a = (a+10) &127;(T22)

FIG. 7B

add \$3, \$1, 10	}(M21)
add \$0, \$3, 255		
add \$4, \$0, 10	}(M22)
add \$0, \$4, 127		

FIG. 7C

uci \$0, \$1, 255(M23)
uci \$0, \$0, 127(M24)

7/18

FIG. 8

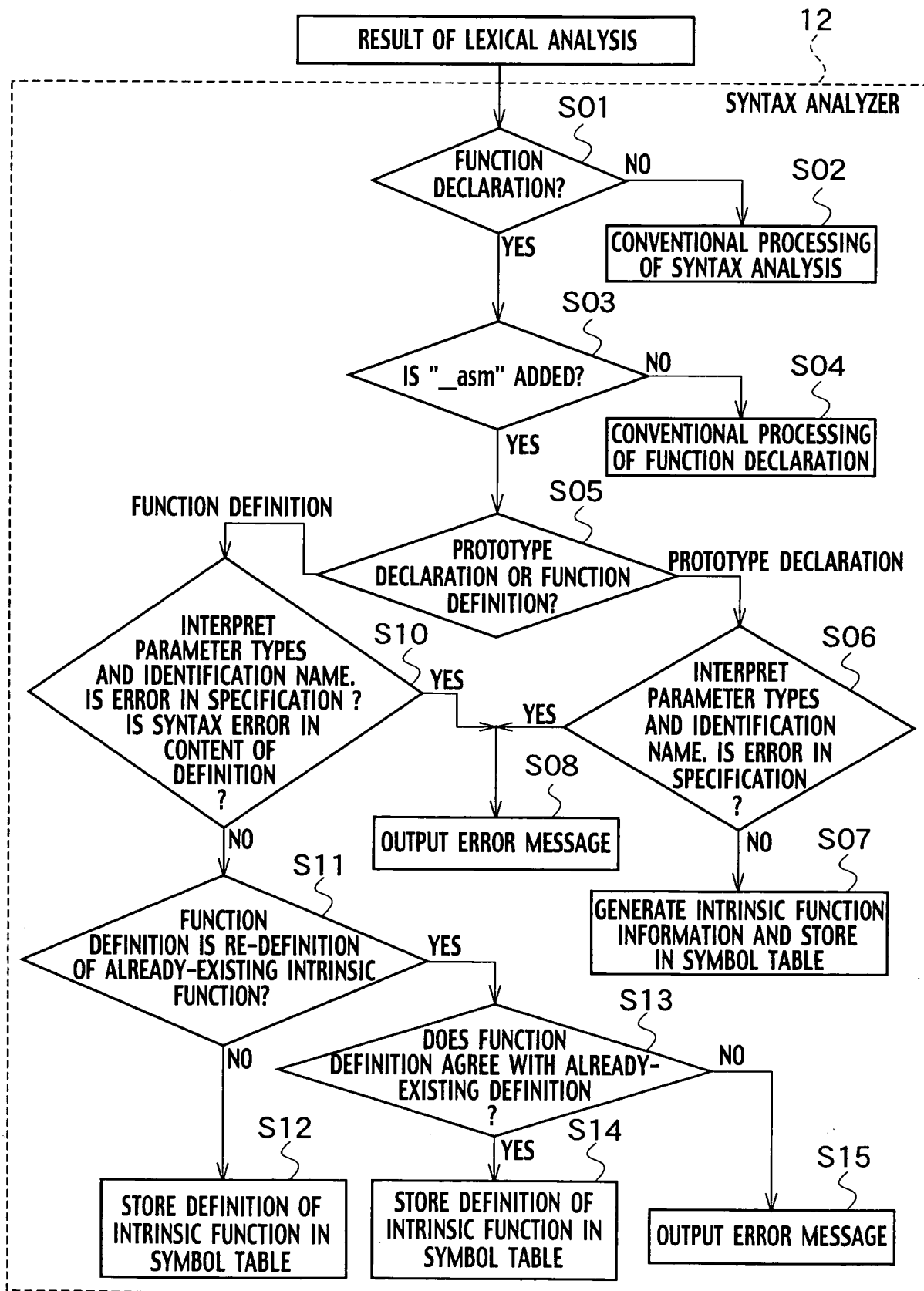
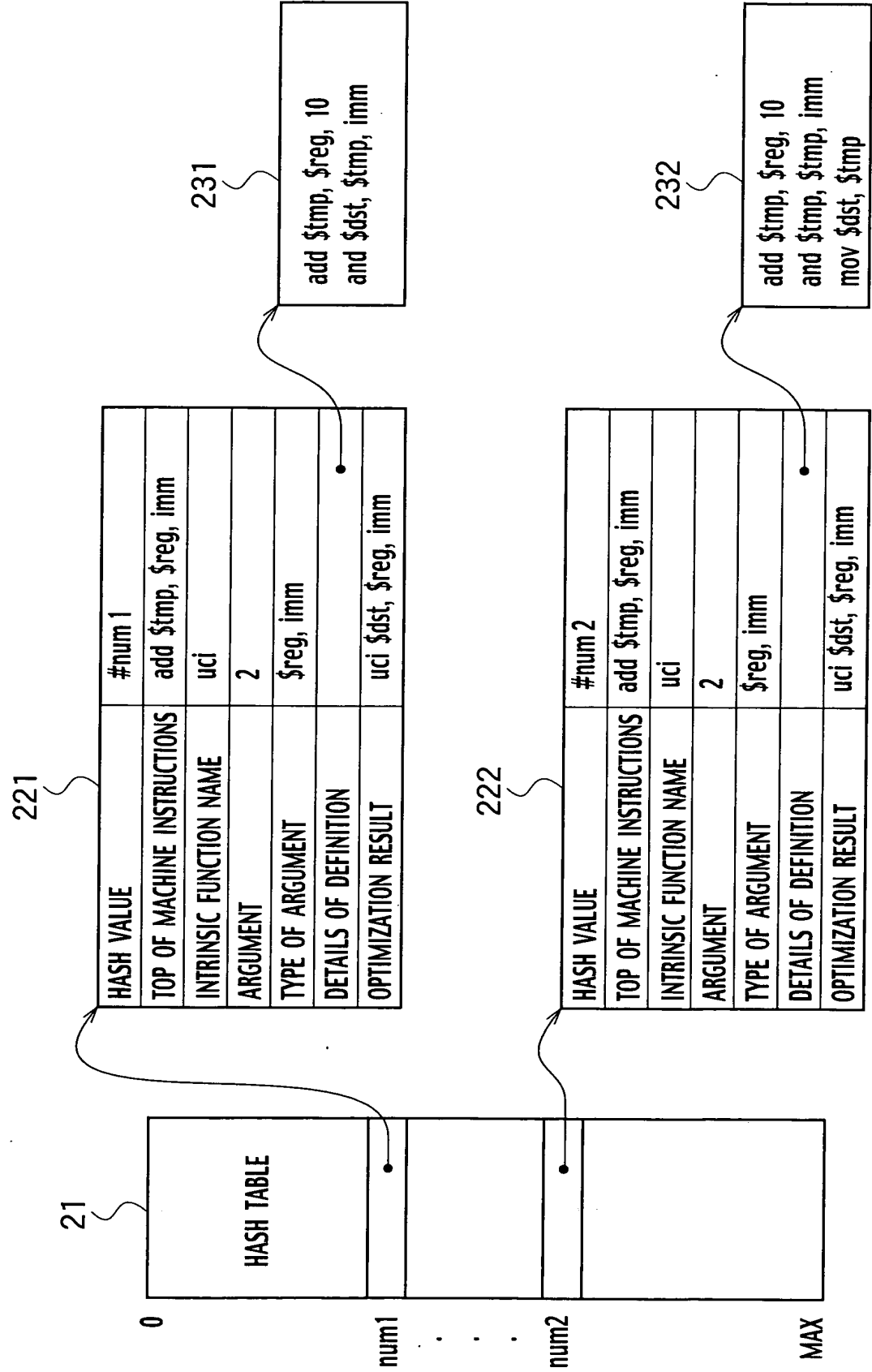
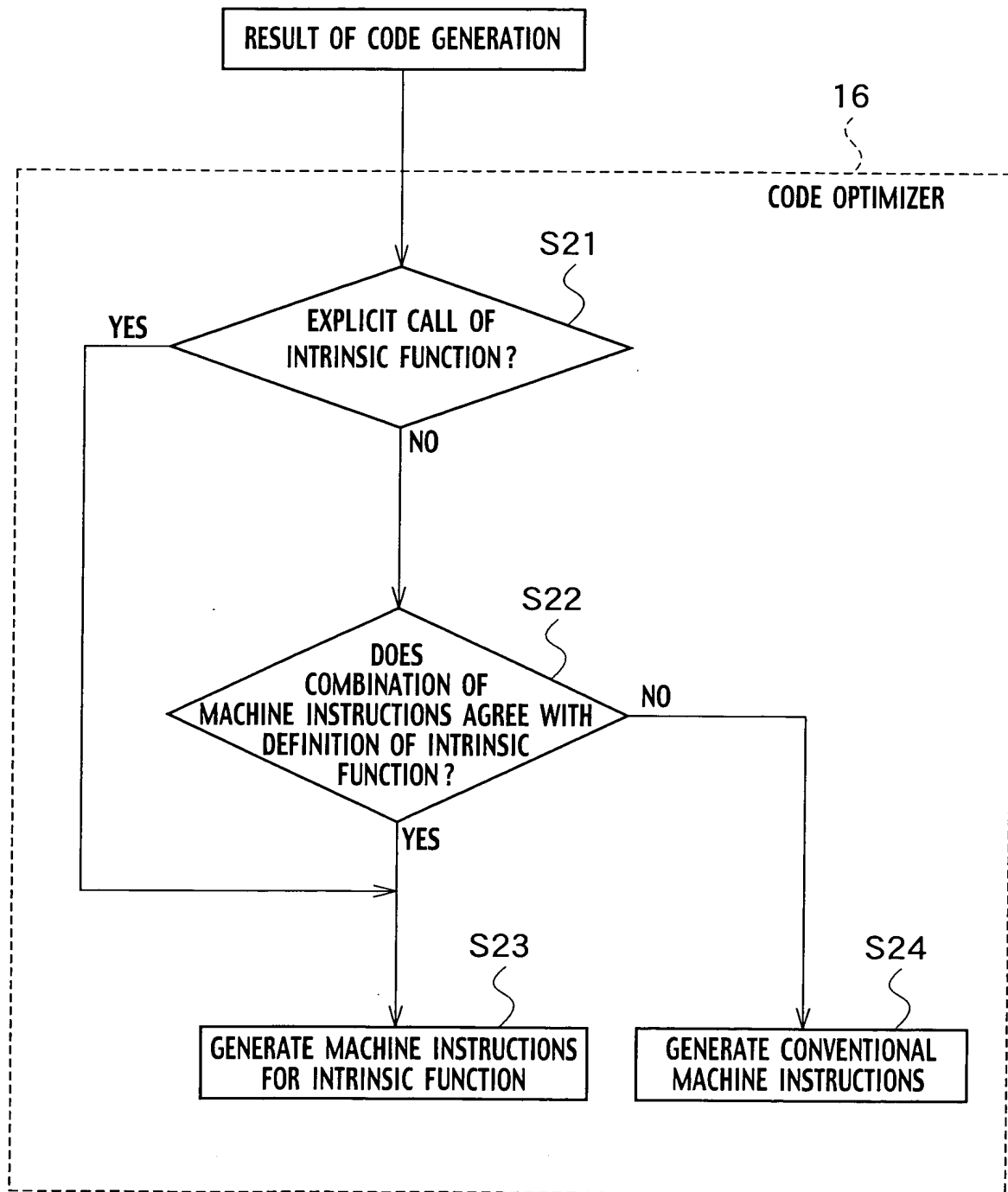


FIG. 9



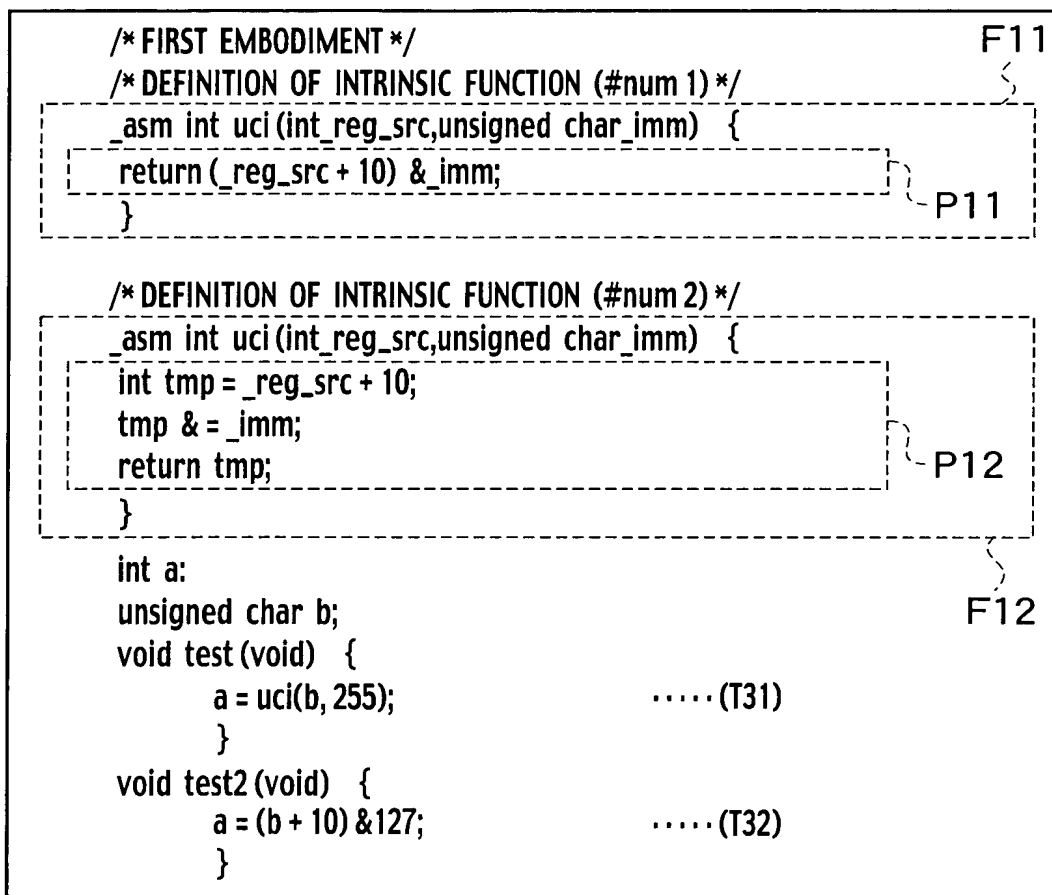
9/18

FIG. 10



10/18

FIG. 11



11/18

FIG. 12

```
_test:
    lbu    $12, %sdaoff(_b) ($14)
    uci    $11, $12, 255                ..... (M31)
    sw     $11, %sdaoff(_a) ($14)
    ret

_test2:
    lbu    $12, %sdaoff(_b) ($14)
    uci    $11, $12, 127                ..... (M32)
    sw     $11, %sdaoff(_a) ($14)
    ret
```

12/18

FIG. 13

```
module uci (  
    meucEUCIcode,  
    meucEUCIRn  
    meucEUCIRm,  
    meucEUCIResult  
);  
input [15:0] meucEUCIcode;  
input [31:0] meucEUCIRn;  
input [31:0] meucEUCIRm;  
output [31:0] meucEUCIResult;
```

P41

```
assign meucEUCIResult  
    = (meucEUCIRm + 32'h0000000a) & { { 16 {1'b0} } , meucEUCIcode } ;  
endmodule
```

13/18

FIG. 14

```
module uci (  
    meucEUCIcode,  
    meucEUCIRn  
    meucEUCIRm,  
    meucEUCIResult  
);  
input [15:0] meucEUCIcode;  
input [31:0] meucEUCIRn;  
input [31:0] meucEUCIRm;  
output [31:0] meucEUCIResult;  
  
wire [31:0] tmp;  
wire [31:0] imm;
```

P42

```
assign tmp = meucEUCIRm + 32'h0000000a;  
assign imm = { {16 {1'b0}} , meucEUCIcode } ;  
assign meucEUCIResult = tmp & imm;
```

```
endmodule
```

14/18

FIG. 15A

```
/* SECOND EMBODIMENT */  
#pragma input HDL add10_and_1.V      ..... (H41)  
#pragma input HDL add10_and_2.V      ..... (H42)  
int a;  
unsigned char b;  
void test(void) {  
    a = uci( b, 255);                ..... (T41)  
}  
void test2(void) {  
    a = (b + 10) & 127;              ..... (T42)  
}
```

FIG. 15B

```
_test:  
    lbu    $12, %sdaoff(_b) ($14)  
    uci    $11, $12, 255              ..... (M41)  
    sw     $11, %sdaoff(_a) ($14)  
    ret  
_test2:  
    lbu    $12, %sdaoff(_b) ($14)  
    uci    $11, $12, 127              ..... (M42)  
    sw     $11, %sdaoff(_a) ($14)  
    ret
```

15/18

FIG. 16

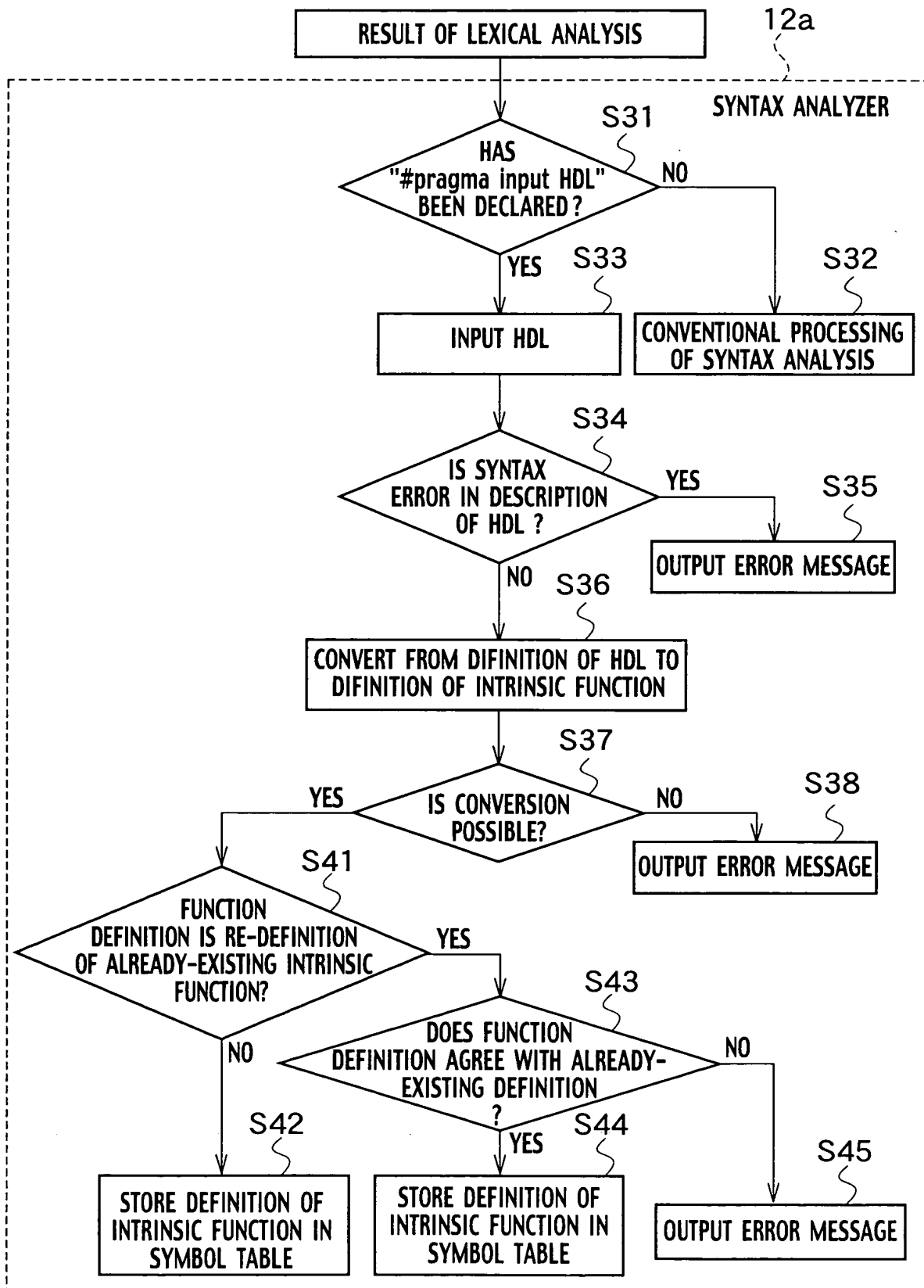
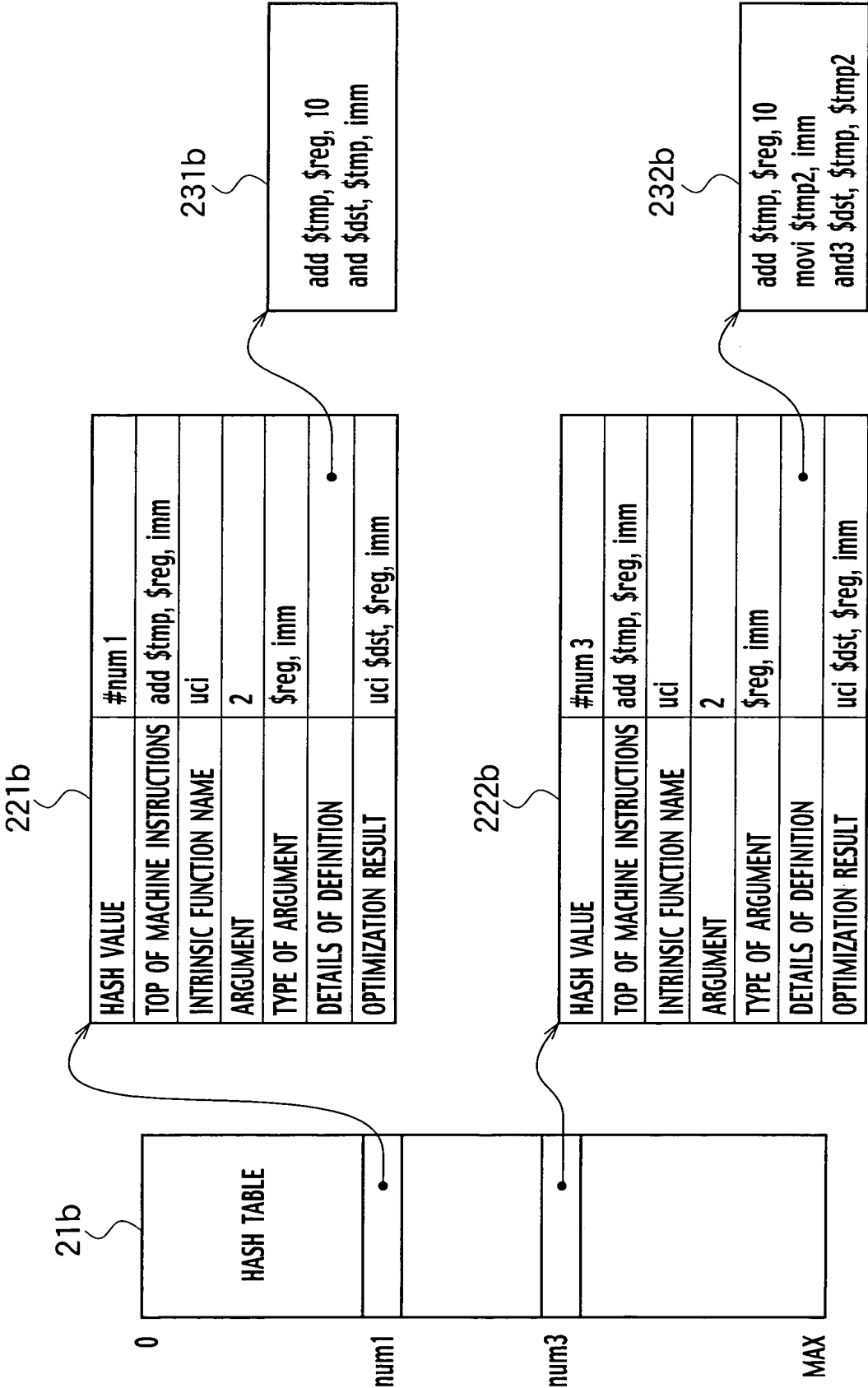
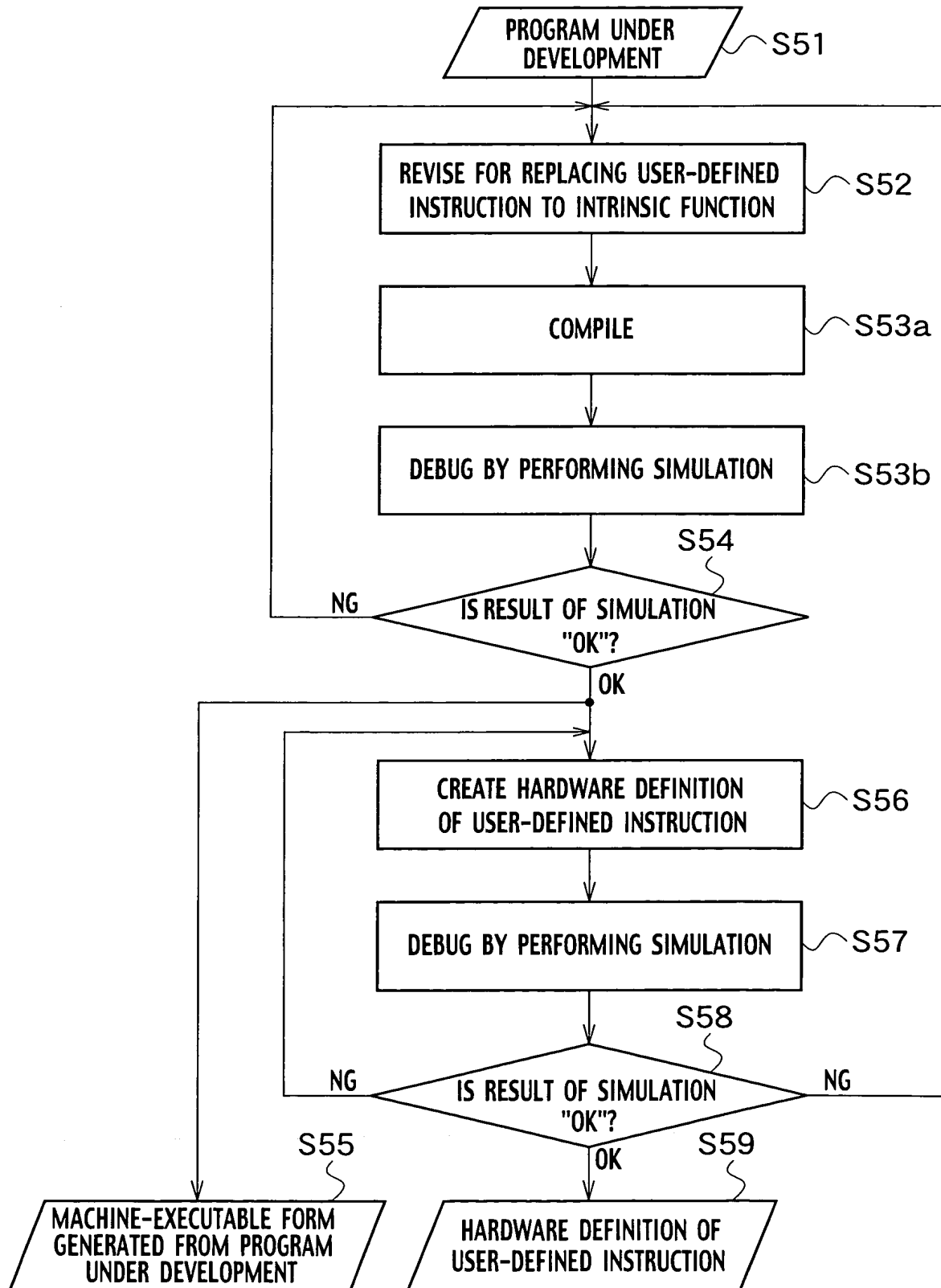


FIG. 17



17/18

FIG. 18



18/18

FIG. 19

